IN THE SPECIFICATION:

Please replace Paragraph [0015] at pages 4, lines 20 - 25, continuing at page 5, lines 1 - 13 with the following corrected, rewritten paragraph.

- - [0015] D.B. Thomasson et al., in an article entitled: "High Mobility Tri-Layer a-Si:H Thin Film Transistors with Ultra-Thin Active Layer", ~~1977~~ 1997 Society for Information Display International Symposium Digest of Technical Papers, volume 28, pages 176 - 179, describe active matrix liquid crystal displays where the TFT has an active layer thickness of about 13 nm. The TFT structure is a glass substrate with a molybdenum bottom electrode, a silicon nitride gate dielectric layer, an a-Si:H layer overlying the silicon nitride gate dielectric layer, n+ μc-Si: H doped source and drain regions, separated by a silicon nitride dielectric mesa, and with an aluminum contact layer overlying each source and drain region. This is referred to as a Tri-layer a-Si:H TFT structure. The authors claim that such hydrogenated amorphous silicon thin-film transistors with active layer thickness of 13 nm perform better for display applications than devices with thicker (50 nm) active layers. The linear (V_{DS} = 0.1V) and saturation region mobility of a 5 μm channel length device is said to increase from 0.4 $cm^2/V \cdot sec$ and 0.7 $cm^2/V \cdot sec$ for a 50 nm a-Si:H device to 0.7$cm^2/V \cdot sec$ and 1.2 $cm^2/V \cdot sec$ for a 13 nm a-Si:H layer device fabricated with otherwise identical geometry and processing. The gate dielectric silicon nitride was deposited from a reactant gas mixture of SiH_4 , NH_3, and AR at 100 mW/cm^2, -150V, 0.5torr and 300 °C. The passivation silicon nitride dielectric layer was deposited at the same conditions as the gate dielectric, with the exception of substrate temperature, which was 250 °C. - -